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CONFIRMATION NO. 3277

SERIAL NUMBER 10/751,523	FILING OR 371(c) DATE 01/06/2004 RULE	CLASS 716	GROUP ART UNIT 2825	ATTORNEY DOCKET NO. 60188-745	
APPLICANTS Takaki Yoshida, Osaka, JAPAN; ** CONTINUING DATA ***** <i>None</i> ** FOREIGN APPLICATIONS ***** JAPAN 2003-034859 02/13/2003 <i>OK</i> IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 04/08/2004					
Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input checked="" type="checkbox"/> Met after Allowance Verified and Acknowledged <i>Kullab</i> Examiner's Signature Initials		STATE OR COUNTRY JAPAN	SHEETS DRAWING 12	TOTAL CLAIMS 11	INDEPENDENT CLAIMS 5
ADDRESS Jack Q. Lever, Jr. McDERMOTT, WILL & EMERY 600 Thirteenth Street, N.W. Washington, DC20005-3096					
TITLE Error portion detecting method and layout method for semiconductor integrated circuit					
FILING FEE RECEIVED 942	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		